59-fJ/bit Si Photonic Crystal Slow-Light Modulator with FinFET-Compatible Driving Voltage

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Abstract: Si Mach-Zehnder modulator with slow-light enhancement of photonic crystal phase shifter consumes a low bit energy of 59 fJ/bit and transmits a 64-Gbaud NRZ signal with a FinFETcompatible driving voltage of 0.87 V.

1. Introduction

High-speed and low-power optical interconnects are used in data centers and high-performance computers. IEEE802.3 400G Ethernet specifies high-speed transmission of over 50 Gbaud, and ongoing development for 800G and 1.6T standards seeks even higher speeds [1]. Optical transmitters for interconnects require high speed, small footprint, low cost, low power consumption, and a wide operating temperature tolerance. For these requirements, CMOS-compatible Si optical modulators offer an attractive solution. Microring modulators have the advantage of a small footprint and low capacitance, which enable low bit energy modulation of several tens of fJ/bit [2], but need temperature control to adjust the resonance to the wavelength, resulting in an additional power penalty and implementation cost. Mach-Zehnder modulators operate in a wide wavelength range and do not require temperature control. Si Mach-Zehnder modulators have a typical $V_{\pi}L$ of 1 V·cm and a phase shifter length of several millimeters, resulting in a bit energy consumption of pJ/bit order [3]. In contrast, Si photonic crystal waveguide (PCW) Mach-Zehnder modulators reduce $V_{\pi}L$ to 1/10 due to the slow light enhancement, thereby achieve a small size and low capacitance [4]. We have introduced meander-line electrodes that eliminate the phase mismatch between slow light and electrical signals and demonstrated 64-Gbps modulation [5]. However, a low termination resistor of 20 Ω and a driving voltage of $V_{\text{pp}} = 3.5$ V were needed for the high-speed modulation. The termination resistor consumes $V_{\rm pp}^2/(4 \cdot R_{\rm T})$ power for push-pull driving, and thus the energy consumption of that device was as high as 2.4 pJ/bit at 64 Gbps. A lower driving voltage and higher resistance were desired to improve the efficiency.

In this study, we demonstrated a highly efficient Si PCW slow-light modulator that consumes a bit energy of only 59 fJ/bit. We introduced a distributed electrode structure to ensure strict electro-optic phase matching and realize high impedance termination. This structure enables successful 64-Gbaud signal transmission at $V_{\text{pp}} = 0.87 \text{ V}$, which provides compatibility with the core voltage of a 12-nm FinFET CMOS process.

2. Device Structure

Fig. 1(a) shows a schematic of the proposed device. The PCW phase shifter is divided into several sections ($N \ge 3$), and transmission lines with a high impedance ($Z_H > 50 \Omega$) are inserted between them. An important advantage of this structure is the improvement of the characteristic impedance. Fig. 1(b) shows the equivalent circuit of the distributed electrode. A high-impedance transmission line can be modeled as a lumped inductor when it is sufficiently short, compared to the wavelength of the RF signal. Similarly, the pn-doped phase shifter with a lower characteristic impedance can be modeled as a lumped RC series circuit. Thus, the electrode can be regarded as a lumped LC ladder circuit like a distributed constant circuit. The effective characteristic impedance of this LC ladder circuit is simply given by $Z_0 = \sqrt{(L_m/C_{pn,seg})}$. Because the high-impedance transmission line increases the inductance of the entire electrode, *Z*⁰ becomes larger than the impedance of the pn-doped phase shifter alone. Fig. 1(c) shows the characteristic impedance of a distributed electrode and a pn-doped phase shifter alone. The phase shifter has an impedance of 35 Ω, while the distributed electrode has $Z_0 = 52 \Omega$. This high impedance allows the driving current to be reduced while maintaining the driving voltage, resulting in low power consumption. Gill et al. [6] reported a similar distributed electrode structure for rib-waveguide-type phase shifters. However, due to the long phase shifter length of rib-type devices, the distributed electrode causes significantly higher RF losses, and the operating speed was limited to 25 Gbaud. In our structure, the phase shifter length is inherently shorter due to the slow-light enhancement, and the distributed electrode can be realized with acceptable RF losses.

Fig. 1. Distributed electrode Si PCW optical modulator. (a) Schematic structure. (b) Equivalent circuit of the electrode. (c) Simulated characteristic impedance. (d) Simulated normalized EO gain. (e) Simulated group delay.

Another benefit of the distributed electrode is a wide bandwidth achieved through strict electro-optic phase matching. To reduce the driving voltage, either the *n*^g or the length of the phase shifter must be increased. However, electro-optic phase mismatch limits the bandwidth. Our previous work has shown that the bandwidth can be improved by dividing the PCW phase shifter into two sections to ensure electro-optic phase matching. Nonetheless, the 3-dB bandwidth was limited to $f_{3dB} = 38$ GHz, even with a low termination resistor of $R_T = 20 \Omega$ [5]. The distributed electrodes ensure strict electro-optic phase matching. As shown in Fig. 1(d), we predicted $f_{3dB} = 39$ GHz by simulation with R_T = 50 Ω for n_g = 20 and a total phase shifter length of 150 µm. In addition, the impedance-optimized distributed electrode suppresses reflections at the termination and achieves excellent group delay response. As shown in Fig. 1(e), the simulated group delay ripple was only 2.3 ps up to 50 GHz. This provides superior jitter performance.

3. Experimental Results

Fig. 2(a) shows a prototype device fabricated using CMOS-compatible 300-mm SOI wafer process. This device has a total footprint of only 0.5 mm \times 0.6 mm = 0.3 mm² including electrodes. Fig. 2(b) shows a measured transmission spectrum. The PCW operates within the wavelength range of 1532–1540 nm. The device exhibited a slightly narrow bandwidth and large loss due to the fabrication errors in the hole size and slab thickness. We performed modulation experiments at the peak wavelength. Laser light of 13 dBm was input into the device through a lensed fiber and endfire coupler. A 64-Gbaud PRBS NRZ signal was generated using a pulse pattern generator and multiplexer. The driving voltage was adjusted by a wideband amplifier, and the amplified signal was input to the device via a GSGSG probe. The output optical signal from the modulator was sent through an EDFA and a 1-nm bandwidth optical filter. We observed the time-series waveforms using a sampling oscilloscope with 65-GHz bandwidth OE module and conducted offline digital signal processing, including resampling and 5-tap symbol-by-symbol adaptive linear equalization. Fig. 2(c) shows the measured BER versus driving voltage, and Fig. 2(d) to (f) show the measured eye diagrams under the conditions indicated in Fig. 2(c). The dashed lines represent the FEC limits and the operating voltage of a 12-nm FinFET CMOS process [7]. We demonstrated 64-Gbaud transmission with BER below the HD-FEC limit at $V_{\text{pp}} =$ 1.57 V compatible with 1.5-V LVCMOS under the quadrature bias condition. Furthermore, we succeeded in meeting the SD-FEC limit at $V_{\text{pp}} = 0.87$ V with a 5-dB deep away from the quadrature bias, which is compatible with the

Fig. 2. Experimental results of the prototype modulator. (a) Top view. (b) Transmission spectrum for Si waveguide transmission. (c) BER versus driving voltage. (d)–(f) 64-Gbaud eye diagrams after 5-tap adaptive linear equalization.

FinFET core voltage. The power consumption of the driving signal was only 3.8 mW, and an excellent power efficiency of 59 fJ/bit was demonstrated.

4. Conclusion

The distributed-electrodes Si PCW slow-light modulator simultaneously achieves high-impedance termination of 50 Ω, and FinFET-compatible driving voltage of 0.87 V. We have demonstrated 64-Gbaud signal transmission with a remarkable power efficiency of 59 fJ/bit without temperature control. These results will lead to the development of ultra-low power optical transceivers.

5 References

[1] https://www.ieee802.org/3/df/index.html

[2] J. Sun et al., "A 128 Gb/s PAM4 Silicon Microring Modulator With Integrated Thermo-Optic Resonance Tuning," J. Light. Technol., **37**, 110–115 (2019).

[3] M. Pantouvaki et al., "Active Components for 50 Gb/s NRZ-OOK Optical Interconnects in a Silicon Photonics Platform," J. Light. Technol., **35**, 631–638 (2017).

[4] H. C. Nguyen et al., "Sub-100 μm Photonic Crystal Si Optical Modulators: Spectral, Athermal, and High-Speed Performance," IEEE J. Sel. Top. Quantum Electron., **19**, 127–137 (2013).

[5] Y. Hinakura et al., "Silicon Photonic Crystal Modulators for High-Speed Transmission and Wavelength Division Multiplexing," IEEE J. Sel. Top. Quantum Electron., **27**, 4900108 (2021).

[6] D. M. Gill et al., "Distributed electrode Mach-Zehnder modulator with double-pass phase shifters and integrated inductors," Opt. Express, **23**, 16857–16865 (2015).

[7] https://www.cmc.ca/globalfoundries-12-lp